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Maria McCormack Sobrino			CHACE, CHRISTIAN	
•	KOLOFF, TAYLOR & Z	ADTIBUT	DARED MUMADED	
Seventh Floor			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	09/977,600	WEBER, WOLF-DIETRICH	
Office Action Summary	Examiner	Art Unit	
	Christian P. Chace	2189	
The MAILING DATE of this communication ap	pears on the cover sheet with the c	orrespondence address	
A SHORTENED STATUTORY PERIOD FOR REPL WHICHEVER IS LONGER, FROM THE MAILING D - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period - Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailin earned patent term adjustment. See 37 CFR 1.704(b).	OATE OF THIS COMMUNICATION 136(a). In no event, however, may a reply be tin will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).	
Status			
1) ⊠ Responsive to communication(s) filed on <u>07 J</u> 2a) ☐ This action is FINAL . 2b) ⊠ This 3) ☐ Since this application is in condition for allowated closed in accordance with the practice under the practice.	s action is non-final. ance except for formal matters, pro		
Disposition of Claims			
4) Claim(s) 1-3,5-11,13,14 and 17-29 is/are pend 4a) Of the above claim(s) is/are withdra 5) Claim(s) is/are allowed. 6) Claim(s) 1-3,5-11,13,14 and 17-29 is/are reject 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers 9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) according and applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Examine 11.	er. cepted or b) objected to by the led drawing(s) be held in abeyance. See cition is required if the drawing(s) is objected to by the led on	e 37 CFR 1.85(a). sected to. See 37 CFR 1.121(d).	
	xammer. Note the attached Office	Action of form 1 10-132.	
Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureat * See the attached detailed Office action for a list	ts have been received. ts have been received in Applicationity documents have been received in (PCT Rule 17.2(a)).	on No ed in this National Stage	
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/12/05.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:		

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7 June 2006 has been entered.

Response to Amendment

This Office action is also responsive to amendment filed 7 June 2006.

Claims 1-3, 5-11, 13-14, and 17-29 are pending. Applicants' arguments have been carefully and respectfully considered, but they are not persuasive.

However, as this is a first action on merit following an RCE, this action has NOT been made final.

Information Disclosure Statement

Examiner wishes to thank applicants fro submitting the missing pages of the reference as discussed in the previous Office action.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before

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the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-11, 13-14, and 17-29 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Strongin et al (US Patent #6,510,497), in view of Novak (WO 01/75620 A1). Novak and Fukuda (US Patent #5,107,257) are also both offered as extrinsic evidence of the inherency of a counter for bus switching. As Fukuda discusses in column 1, lines 24-26, bus switching by counting accesses prevents having to utilize a looped bus.

After careful consideration of applicants' instant remarks, it appears there is some disagreement as to whether a counter is inherent to Strongin et al – that is, a counter necessarily flows from the rest of the disclosure of Strongin et al. Given these discussions, examiner believes that a prima facie case has been made for the inherency of the counters in the Strongin et al reference.

However, assuming arguendo that one were to be able to interpret the claims differently and not find the counter inherent in the system of Strongin et al, Novak clearly discloses the counter and the motivation for it's inclusion in a system at least equivalent to the Strongin et al system in at least page 6, lines

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23-33, which recites that the number of page hit requests serviced consecutively has to be limited to prevent starvation of the other devices, and that this is accomplished through counting the number of requests up to a threshold, set to be from 1 to 32 requests.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the counter and threshold of Novak in the system of Strongin et al to prevent starvation of the other devices, as discussed by Novak on page 6 at line 25.

It is noted that a counter inherently stores a "switch point," and is inherently "dynamically" configurable.

In addition, with specific respect to claim 21, which invokes interpretation under 35 USC 112, 6th paragraph, applicants' instant remarks appear to indicate that this claim should be interpreted in it's broadest reasonable sense, as applicants appear under the impression that they are not required to point out the corresponding structure in the instant specification, but merely offer an example of a structure that could perform the functions. (See page 8 of instant remarks). Accordingly, it is unclear how the claims should be interpreted under 35 USC 112, 6th paragraph.

Does the corresponding structure in Strongin et al need to be equivalent to that of any or all of the examples offered in the instant specification? Examiner believes that it does not, and the "broadest reasonable" interpretation is appropriate herein.

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However, should one argue that Strongin et al does not have corresponding equivalent structure disclosed to that of the instant specification to be anticipatory, certainly the Strongin et al structure is obvious, at least because it is performing the same functions as recited in the instant claims, (also for the same reasons – decrease in latency, see Strongin et al column 12, lines 52-54, e.g.), as is discussed below with respect to at least claim 1; a person of ordinary skill in the art would have recognized the interchangeability of the element shown in the prior art for the corresponding elements disclosed in the instant specification; and that there are insubstantial differences between the applied reference's structure and the examples offered in the instant specification.

Given the discussions supra, the anticipatory rejections are as follows with respect to Strongin et al:

With respect to independent claims 1 and 21, a method for scheduling access to a device is disclosed in the title.

As a result of applicants' instant arguments as discussed supra, claim 21 has been interpreted in it's broadest reasonable sense, as no specific structural means further narrowing the claimed "means" appear to be disclosed – mere examples do not further limit the structure. See MPEP 2181-2184.

Tracking a current state of the device is disclosed in column 11, lines 45-50. This is also disclosed in column 18, lines 22-35 as "determining a status."

Tracking a count of a number of scheduled (i.e., in the buffer) requests which require the current state is disclosed in column 11, lines 55-60, as the number of requests issued and/or amount of time elapsed. Both current and

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future states would inherently require a count of some sort. A count is one or more, and the particular state is the bus direction, e.g., as is further explained in column 18, lines 22-35. In addition, column 4, line 20 discloses scheduling "one or more requests." Counting the number of those requests necessarily flows from the Strongin et al reference as it could not operate without knowing how many requests there are. In addition, should the number of requests not be counted, then starvation of all but the one device that starts using it would have to occur, because nothing would prevent it from happening. Also, the system knows how many requests are issued per unit time (it must in order to operate). Therefore, it is also known the number of requests issued of the amount of time is known.

Switching the state of the device after determining the count reaches a threshold value established for a switch point (number of pending operations) and receiving one or more incoming requests which require an alternate state to the current state (a different bus direction or a different open bank of DRAM) of the device is disclosed in column 12, lines 20-35. Also see column 18, lines 22-35, which discusses scheduling a number of "tracked" requests based on the bus direction, or "device state." The "switch point" is when the pending requests consistent with the memory bus direction are issued, and the bus direction reverses, or switches, to allow the scheduled requests that were previously inconsistent with the previous bus direction to now issue. However many requests there are, in a certain bus direction (read or write), in the queue, is the threshold.

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With respect to claims 2 and 7, "configuring" the switch point is disclosed in column 12, lines 22-33, which is the number of pending requests. As this number changes, the switch point is "re-configured."

With respect to claims 3 and 12, the switch point being configurable by software is disclosed in column 15, lines 5-10. As discussed with respect to the independent claims upon which the instant claims depends, e.g., claim 1, the switch point is configurable. Strongin et al clearly discuss hardware and software being interchangeable.

With respect to claims 4 and 9, the switch point being "dynamically" configurable is discussed supra with respect to claims 2 and 7. "Dynamic" simply means it changes.

With respect to claims 5 and 11, the device being a DRAM is disclosed in column 13, line 8, for example. The method further comprising selecting a scheduler type from the group consisting of a DRAM bus turnaround scheduler (consistent with the direction of a bus), DRAM page scheduler (targeted to one or more open pages in memory), and DRAM physical bank switching scheduler (identifying one or more closed pages, such as banks, in column 13, lines 50-67, for example) is disclosed in column 14, lines 20-60. In addition, see column 12, lines 11-44.

With respect to independent claim 6, a bus scheduler is disclosed in column 17, line 4 as an arbiter configured to arbitrate between memory requests according to a bus direction.

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An input configured to receive at least one incoming request, each request indicating a bus direction is disclosed in column 18, lines 22-35, which discloses pending memory access commands, which are scheduled based on their consistency or lack thereof with the memory bus direction. Inherently, there must be an "input configured to receive" these requests for the system to operate – a computer must be told what to do.

A switch point is disclosed in column 18, lines 22-35 in that the "switch point" is when the first set of pending requests are issued and the bus direction switches to accommodate the second set of pending request that were previously inconsistent with that bus direction.

An indicator of a current bus direction is disclosed in column 18, lines 22-35 and in lines 55-60, which discusses determining the direction of the bus.

Inherently, if the bus direction is determined, it is indicated.

A count of requests processed through the current bus direction is disclosed in column 18, lines 22-35 as the "one or more" pending access requests. "One or more" indicates a number, which is a count.

Logic configured to switch the direction of the bus to process incoming requests after the count reaches the switch point and there are incoming requests having the direction opposite to the current direction of the device bus is disclosed in column 18, lines 22-35, which discloses issuing the requests consistent with a bus direction ahead of, or before, the requests inconsistent with the bus direction. (The logic for implementing this method is disclosed in column 17 and 18 in claims 1-12, for example).

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With respect to independent claim 8, a scheduler is disclosed as a memory arbiter in column 17, line 4.

A switch point is disclosed as discussed supra with respect to claims 1 and 6.

A current device state is disclosed as a bus direction and/or a page status in column 18, lines 22-35.

A count is disclosed as "one or more" in column 18, line 30.

Logic configured to "facilitate" an updated device state when the count crosses a threshold of the switch point is disclosed in column 18, lines 22-35, where memory accesses are scheduled based on the bus direction and the page status.

Scheduling the access requests to the device using the updated device state is disclosed in column 18, lines 22-35, which discloses that after the pending requests that are consistent with the device state are issued, the access requests are then issued ("ahead of") that are inconsistent with the previous device state.

With respect to claim 10, the device comprising a bus and the device state comprising a bus direction, said scheduling being dependent upon the bus direction is disclosed in column 11, lines 64-65.

With respect to claim 13, the device comprising a DRAM with multiple pages and the device state comprising the identity of at least one open page, said scheduling being dependent upon the at least one page opened is disclosed in column 11, lines 5-10.

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With respect to claim 14, the device comprising a DRAM with multiple physical banks and the device state comprising the last accessed physical bank, said scheduling dependent upon the last accessed physical bank is disclosed in column 15, lines 29-34.

With respect to claims 17-18, a system on a chip, or ASIC, is disclosed in column 14, line 60 into column 15, line 11.

With respect to claims 19-20, a controller of a volatile memory coupled to the scheduler (via the bus) is disclosed in figure 6, #400, e.g.

Claims 22-29 are clearly anticipated by Strongin et al, as discussed supra with respect to the claims upon which they depend.

Filter logic is disclosed in figure 6, #482. It may inherently be configured to do anything. However, one or more threads are disclosed in figure 6, #486 – 1,2, D, e.g., as a thread goes through each, as discussed in column 13, lines 16-38. As discussed in the previous rejection, the "based on...for each thread" is merely an intended result of the actual structure and operation, and, accordingly, will not be given weight. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function alone. MPEP 2114.

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strongin et al (cited supra). Examiner notes that this has been taken as admitted prior art in accordance with MPEP, as applicants have not traversed the taking of Official Notice in the previous Office action.

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With respect to claims 15-16, Strongin et al recite the subject matter of the claims upon which the instant claims depend, as discussed supra.

The difference between the explicit recitation of Strongin et al and the instant claims, is the explicit recitation of a register to store the threshold number of counts to establish a switch point.

It is extremely well known to those of even rudimentary skill in the art that a register may be employed to count requests in a buffer or queue of requests to inform the system of how many particular requests may be present. The examiner takes OFFICIAL NOTICE of this teaching.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Strongin et al before him/her, to utilize a counter (register) to count the number of requests using a certain bus direction, so the system would know how long to keep the bus going in that certain direction so that service may be provided in the round-robin format discussed by Strongin et al in column 10, lines 27-42, e.g.

Claim Rejections - 35 USC § 102

Claims 1-3, 5-11, 13-14, and 17-29 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Novak (cited supra).

Page 4 discloses a DRAM, which is a non-volatile memory. Page 6, lines 2-3, disclose page mode accesses as page hit requests, page miss requests, page miss different chip requests, and page conflict requests. These are the device states. Priority logic block is disclosed at page 6, lines 7-8. Page 6, lines 23-33 discuss the prioritization of the requests wherein a certain preset

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(dynamically configured and stored) number of page hit requests will be issued sequentially to reduce the latency of the system and enhance the utilization of the memory bus, as is disclosed in the abstract.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571.272.4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christian P. Chace Primary Examiner Art Unit 2189